MICROPROGRAM CONTROL UNIT (MCU)

5710/6710

Preliminary Product Specifications

Monolithic Memories INCORPORATED

PRODUCT FEATURES

- **Address 512 Word Pages of Memory**
- **8 Control Functions**
- **Microsubroutine Capability**
- **On-Chip Sequence Counter**
- **6 Flag Branch Inputs**
- **4-Way Branching**

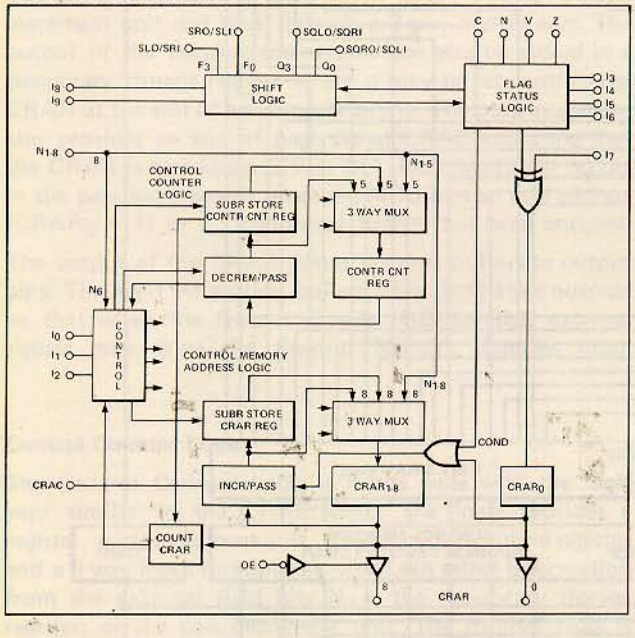
PRODUCT NUMBER

Temperature Range	Product Number
Military	5710
Commercial	6710

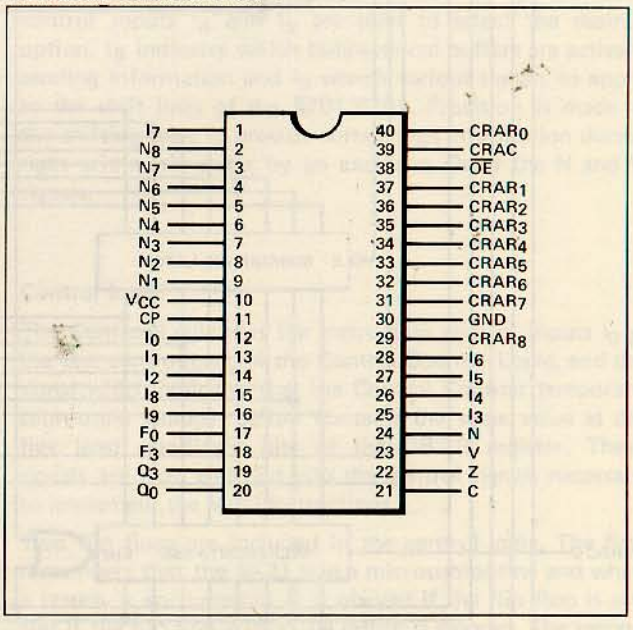
DESCRIPTION

The 5710/6710 Microprogram Control Unit (MCU) is a member of the 5700/6700 Computer Logic family of high performance bipolar compatible Schottky TTL components. The device is designed to work in conjunction with the 5701/6701 4-bit slice microcontroller and standard ROMs and PROMs for the design of extremely powerful computing systems. The power and flexibility of the MCU also allow it to be used for general purpose control applications. The MCU can directly address up to 512 words of microprogram control memory; larger memories can be accommodated using simple paging techniques. One of up to six flag signals can be selected from the 5701/6701 to provide two way conditional branching at every step in a microprogram on the value of the flag or its stored value. Four way conditional branches are possible using an on-chip control counter. The MCU has 8 instructions including continue, conditional and unconditional jumps, conditional and unconditional subroutine jumps to a single level subroutine and subroutine return. Connections are provided to the 5701/6701 for a minimum set of shifting options. The MCU is a synchronous device using a single clock and can operate in systems with less than a 100 ns microinstruction period. The device uses a single +5 V power supply and is packaged in a standard 40 pin DIP.

BLOCK DIAGRAM



PIN CONFIGURATION

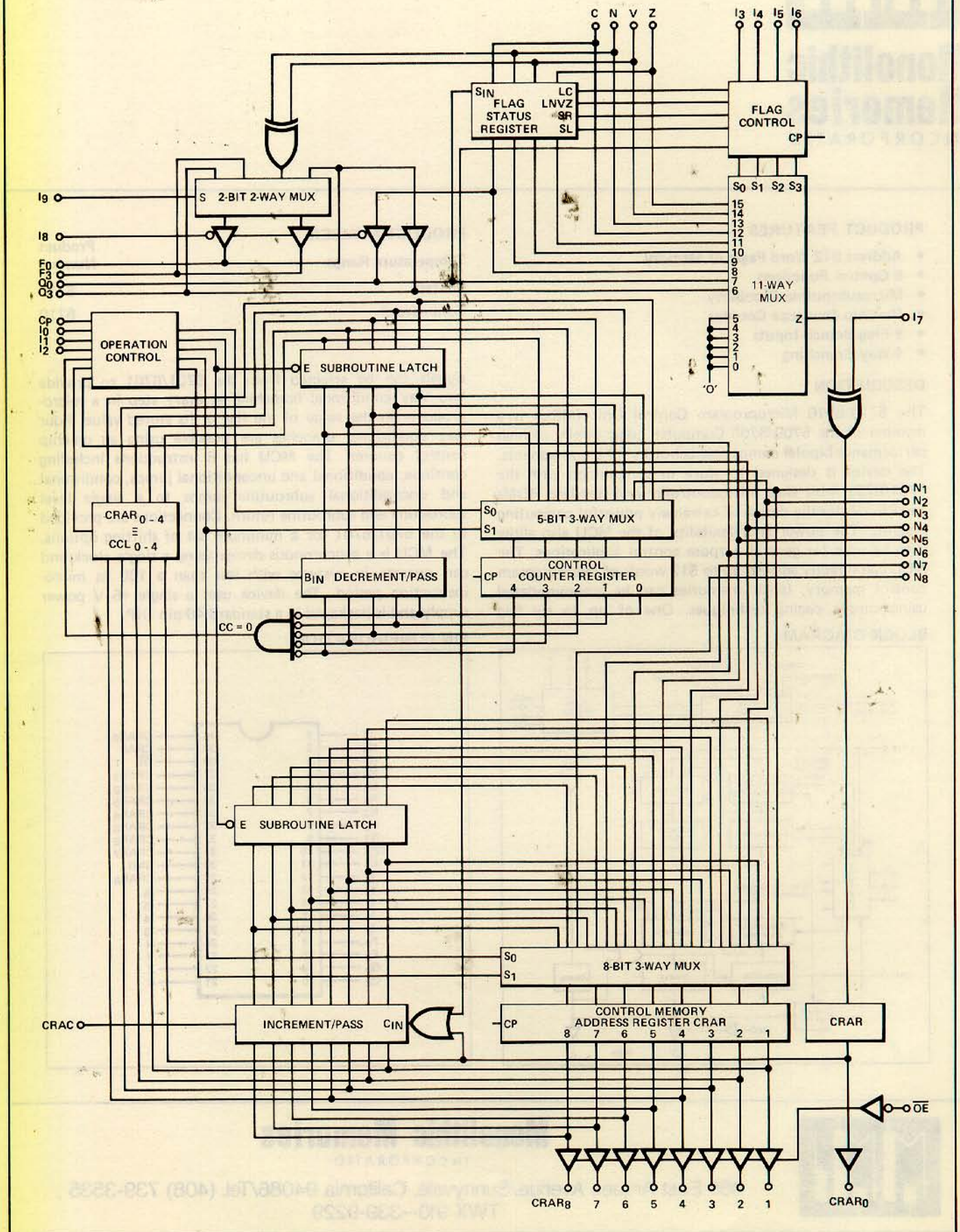


Monolithic Memories INCORPORATED

1165 East Arques Avenue/Sunnyvale, California 94086/Tel. (408) 739-3535

TWX 910—339-9229

5710/6710 DETAILED BLOCK DIAGRAM



DETAILED DESCRIPTION

The MCU is a synchronous machine. All changes visible on external pins occur on the single clock Low to High transition. Internally there are both dual rank registers (flip flops) and single rank registers (latches). The latches are enabled when the clock is Low and this together with some inputs defining information destinations causes timing constraints, such that certain input signals must not change while the clock is Low. These timing constraints are shown in the timing diagrams.

The MCU can be divided up into a number of sections. These sections are the Control ROM Address Register ($CRAR_{0-8}$) Logic, the Control Counter (CC) Logic, the Flag Status Logic, the Shifting Control for the 5701/6701 and the MCU Control Logic.

CRAR Logic

The CRAR is split up into two sections, an eight bit section which can remain unchanged, be incremented, loaded from a subroutine temporary storage register latch and loaded from an 8-bit external field N_{1-8}. The one bit section is the least significant bit of the Address Word and is directly driven from the output of the Flag Status Logic. The output of the Flag Status Logic therefore defines whether the next address is even or odd depending upon the condition of the selected flag signal. This allows two way branching at every clock period.

The eight bit section of the register passes through a pass/increment unit and back through a 3-way multiplexer. The output of the pass/increment unit can also be stored in a temporary storage register where it may be returned to the CRAR at the end of a microsubroutine. The pass/increment also provides an end of page signal CRAC indicating that the CRAR is at address 510 or 511. Incrementation occurs in the pass/incrementor when the MCU is at an odd address ($CRAR_0 = 1$) or a Conditional Branch has been selected.

The output of the CRAR passes through buffers to output pins. The eight bit section buffers have three state outputs so that when the Output Enable ($\overline{OE}$) is High external signals may drive the Control Memory Address lines.

Control Counter Logic

The Control Counter Logic is 5 bits wide with the logic very similar to the CRAR logic. The logic includes a register, pass/decrement unit, temporary subroutine register and a 3-way input multiplexer which can select information from the external field bits N_{1-5}, the temporary storage register, or the pass/decrement unit. The counter logic is used during the two conditional jump instructions. Each time the MCU encounters a conditional jump instruction the control counter register is tested for zero and decremented. If the register was zero then the MCU instead of performing a Jump instruction continues on to the next address pair. The next time the conditional jump instruction occurs the procedure is repeated but now the value of the register is one less. The control counter register can be loaded from the N_{1-5} inputs on receipt of a Continue Load Control Counter instruction.

Flag Status Logic

The Flag Status Logic consists of a loadable Shift Left/Shift Right register, an eleven way multiplexer, an exclusive Or gate and a small amount of control logic. The shift register can be loaded with four flags C, N, V, Z, with separate loading selection for C and the group NVZ. The register can be shifted one place Left with N going to C, V to N, etc., and a logic zero being pulled into Z. The C register bit is placed on the bidirectional input/output line Q_0 and would most likely in a system enter the least significant bit of the Q register in the 5701/6701. A Right shift causes C to be loaded from Q_0 this time acting as an input, and what is in C going to N, etc.

The eleven way multiplexer can be used via the select and control lines I_{3-6} to select one of the following signals: Stored C, N, V, Z, Present C, N, V, Z, logic 0, Q_0 and Q_3. All of these signals can be inverted by having $I_7 = 1$, enabling branching on $\overline{C}$, $\overline{N}$, etc. The output of the Flag Status Logic Ex Or gate is the input to the least significant CRAR register bit. The Flag Status Logic also provides a signal to the pass/increment unit to indicate that a conditional branch is present and the unit should increment.

Shift Control Logic

The Shift Control Logic provides the connections for a minimum set of useful 5701/6701 shifting options. Two control inputs I_8 and I_9 are used to select the desired option. I_8 indicates which bidirectional buffers are actively sending information and I_9 selects various signals to apply to the shift lines of the 5701/6701. Provision is made in the shifting logic to provide correct sign information during right arithmetic shifts by an exclusive Or of the N and V signals.

Control Logic

The Control Logic uses the instruction control inputs I_{0-2}, the test zero output of the Control Counter Logic, and the signal which indicates that the Control Counter temporary subroutine storage register contains the same value as the five least significant bits of the CRAR register. These signals are then encoded into the control signals necessary to implement the MCU instructions.

Two flip flops are included in the control logic. The first remembers that the MCU is in a microsubroutine and when a return is encountered it is obeyed if the flip flop is set, and if the flip flop is clear the return is ignored. The second flip flop indicates that a Preprogrammed Return Subroutine is in progress called by instruction 101, and the MCU should automatically return when equivalence of the CRAR and CC subroutine latch is achieved. Both these flip flops are automatically cleared during power on and may be reset under microprogram control by loading the Control Counter with $N_6 = 1$.

Table I — MCU Control Options

Control Code			Address Field Destination	Control Action
I_2	I_1	I_0		
0	0	0	None	Continue to next μinstruction
0	0	1	Control Counter	Continue to next μinstruction
0	1	0	None/CRAR (Cond. Jump)	Jump to next μinstruction if Control Counter ≠ 0, Decrement Control Counter
0	1	1	None/CRAR (Cond. Subr. Jump)	Subroutine Jump to next μinstruction if Control Counter ≠ 0, Decrement Control Counter
1	0	0 *	None	Return from Subroutine
1	0	1 **	CRAR (Jump Subroutine)	Jump to next μinstruction Return from Subroutine when Control Counter Subroutine Latch ≡ $CRAR_{0\text{-}4}$
1	1	0	CRAR (Jump)	Jump to next μinstruction
1	1	1	CRAR (Jump Subroutine)	Subroutine Jump to next μinstruction

* The machine will only return to the calling program if it entered a Subroutine via a Subroutine Jump instruction; otherwise it will continue to the next μinstruction in sequence.

** This operation allows the Controller to branch to a section of code, perform the operations outlined by the code and return after a preprogrammed CROM address has been reached or if a return is encountered.

Table II — Flag Status Control Options

Control Code				Action		
I_6	I_5	I_4	I_3			
0	0	0	0	None	I_7 to $CRAR_0$	Unconditional Branch
0	0	0	1	Store C	I_7 to $CRAR_0$	Unconditional Branch
0	0	1	0	Store N, V, Z	I_7 to $CRAR_0$	Unconditional Branch
0	0	1	1	Store C, N, V, Z	I_7 to $CRAR_0$	Unconditional Branch
0	1	0	0	Shift Flag Register into Q_0	I_7 to $CRAR_0$	Unconditional Branch
0	1	0	1	Shift Flag Register out of Q_0	I_7 to $CRAR_0$	Unconditional Branch
0	1	1	0	Instantaneous value of Q_3 to $CRAR_0$		Conditional Branch
0	1	1	1	Instantaneous value of Q_0 to $CRAR_0$		Conditional Branch
1	0	0	0	Stored value of C to $CRAR_0$		Conditional Branch
1	0	0	1	Stored value of N to $CRAR_0$		Conditional Branch
1	0	1	0	Stored value of V to $CRAR_0$		Conditional Branch
1	0	1	1	Stored value of Z to $CRAR_0$		Conditional Branch
1	1	0	0	Instantaneous value of C to $CRAR_0$		Conditional Branch
1	1	0	1	Instantaneous value of N to $CRAR_0$		Conditional Branch
1	1	1	0	Instantaneous value of V to $CRAR_0$		Conditional Branch
1	1	1	1	Instantaneous value of Z to $CRAR_0$		Conditional Branch

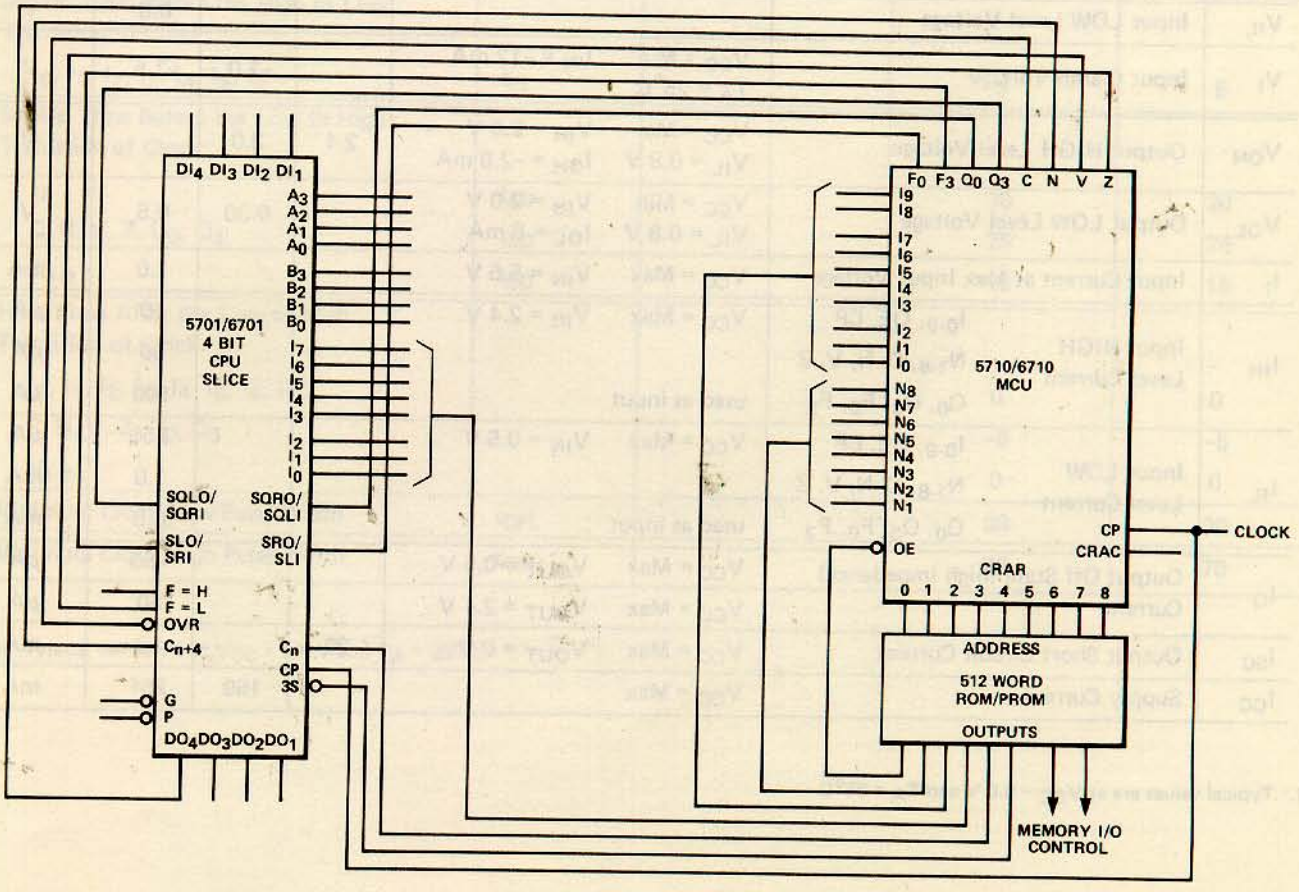
Code bit I_7 inverts the status of output line so that the condition is dependent upon $\overline{C}$, etc. For the first six entries in the table if $I_7 = 0$ there is an unconditional branch to X,0. If $I_7 = 1$ an unconditional branch to X,1.

Table III – Shift Control

Control Code		Shifting Operation	Bidirectional Shift Lines Acting as Outputs			
			F_3 (SLO/SRI)	F_0 (SRO/SLI)	Q_3 (SQLO/SQRI)	Q_0 (SQRO/SQLI)
I_9	I_8					
0	0	Arithmetic Shift Left	–	Q_3	–	Flag (SC)
0	1	Arithmetic Shift Right	N⊕V	–	F_0	–
1	0	Rotate Shift Left	–	F_3	–	Flag (SC)
1	1	Rotate Shift Right	F_0	–	–	–

– High Impedance State
SC Contents of Carry Flip Flop

5710/6710-5701/6701 INTERCONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5 to +7 V
Input Voltage	-1.5 to +5.5 V
Output Current	100 mA
Ambient Temperature	-55 to +125°C
Storage Temperature	-65 to +150°C

Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is not guaranteed or implied.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

6710	T_A = 0°C to +70°C	V_{CC} = 5.0 V ± 5%	Min = 4.75 V	Max = 5.25 V
5710	T_A = -55°C to +125°C	V_{CC} = 5.0 V ± 10%	Min = 4.5 V	Max = 5.5 V

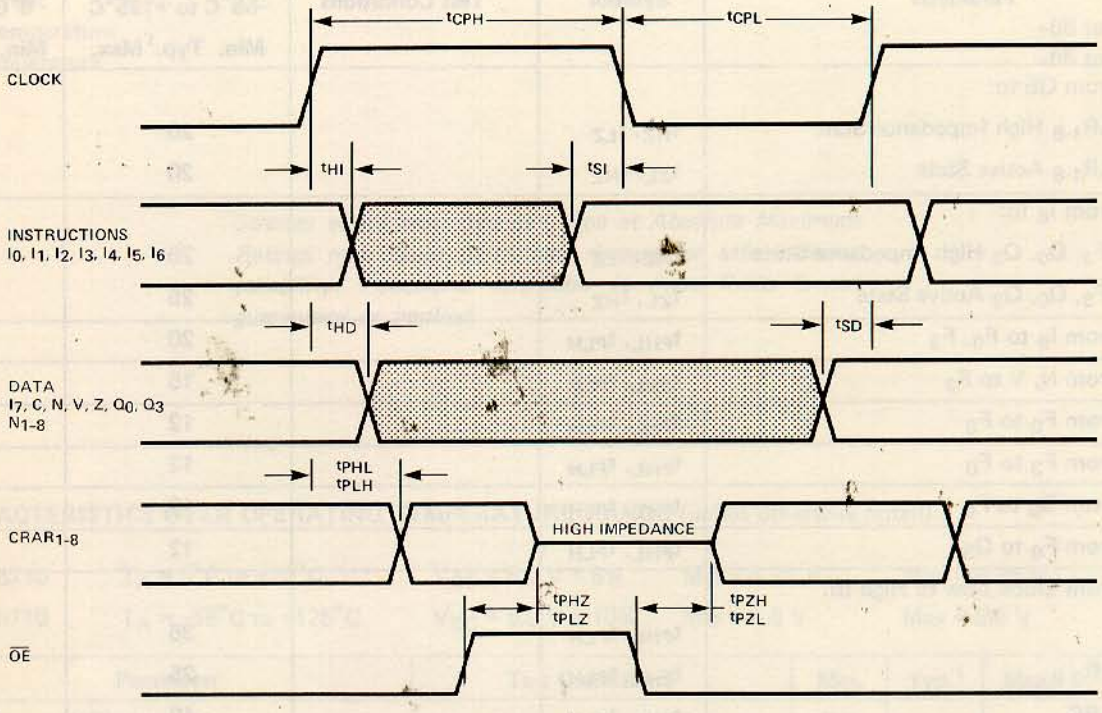
Symbol	Parameter		Test Conditions		Min.	Typ.[1]	Max.	Units
V_{IH}	Input HIGH Level Voltage				2.0			V
V_{IL}	Input LOW Level Voltage						0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min T_A = 25°C	I_{IN} = -12 mA		-1.0	-1.5	V
V_{OH}	Output HIGH Level Voltage		V_{CC} = Min V_{IL} = 0.8 V	V_{IH} = 2.0 V I_{OH} = -2.0 mA	2.4	3.0		V
V_{OL}	Output LOW Level Voltage		V_{CC} = Min V_{IL} = 0.8 V	V_{IH} = 2.0 V I_{OL} = 8 mA		0.30	0.5	V
I_I	Input Current at Max Input Voltage		V_{CC} = Max	V_{IN} = 5.5 V			1.0	mA
I_{IH}	Input HIGH Level Current	I_{0-9}, OE, CP	V_{CC} = Max	V_{IN} = 2.4 V			10	µA
		N_{1-8}, C, N, V, Z					50	µA
		Q_0, Q_3, F_0, F_3	used as input				100	µA
I_{IL}	Input LOW Level Current	I_{0-9}, OE, CP	V_{CC} = Max	V_{IN} = 0.5 V			250	µA
		N_{1-8}, C, N, V, Z					1.0	mA
		Q_0, Q_3, F_0, F_3	used as input				0.5	mA
I_O	Output Off State (high impedance) Current		V_{CC} = Max	V_{OUT} = 0.5 V			-50	µA
			V_{CC} = Max	V_{OUT} = 2.4 V			50	µA
I_{SC}	Output Short Circuit Current		V_{CC} = Max	V_{OUT} = 0 V	20		90	mA
I_{CC}	Supply Current		V_{CC} = Max			159	254	mA

1. Typical values are at V_{CC} = 5.0 V and T_A = 25°C.

AC CHARACTERISTICS

Parameter	Symbol	Test Conditions	5710 5 V ± 10% V_{CC} -55°C to +125°C			6710 5 V ± 5% V_{CC} 0°C to +75°C		
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.
Delay from OE to:								
$CRAR_{1-8}$ High Impedance State	t_{HZ}, t_{LZ}				20			20
$CRAR_{1-8}$ Active State	t_{ZL}, t_{HZ}				20			20
Delay from I_8 to:								
F_0, F_3, Q_0, Q_3 High Impedance State	t_{HZ}, t_{LZ}				25			25
F_0, F_3, Q_0, Q_3 Active State	t_{ZL}, t_{HZ}				25			25
Delay from I_9 to F_0, F_3	t_{PHL}, t_{PLH}				20			20
Delay from N, V to F_3	t_{PHL}, t_{PLH}				15			15
Delay from F_0 to F_3	t_{PHL}, t_{PLH}				12			12
Delay from F_3 to F_0	t_{PHL}, t_{PLH}				12			12
Delay from Q_0 to F_0	t_{PHL}, t_{PLH}				12			12
Delay from F_0 to Q_3	t_{PHL}, t_{PLH}				12			12
Delay from Clock Low to High to:								
Q_0	t_{PHL}, t_{PLH}				35			35
$CRAR_{0-8}$	t_{PHL}, t_{PLH}				25			25
CRARC	t_{PHL}, t_{PLH}				40			40
Set-Up Time Before the High to Low Transition of Clock:								
I_0, I_1, I_2, I_3, I_4, I_5, I_6	t_{SI}				5			5
Set-Up Time Before the Low to High Transition of Clock:								
I_7	t_{SD}				20			20
C, N, V, Z, Q_0, Q_3	t_{SD}				25			25
N_{1-8}	t_{SD}				15			15
Hold Time After the Low to High Transition of Clock:								
I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7					0			0
C, N, V, Z, Q_0, Q_3					-5			-5
N_{1-8}					0			0
Minimum Clock Low Pulse Width	t_{CPL}				30			30
Minimum Clock High Pulse Width	t_{CPH}				70			70

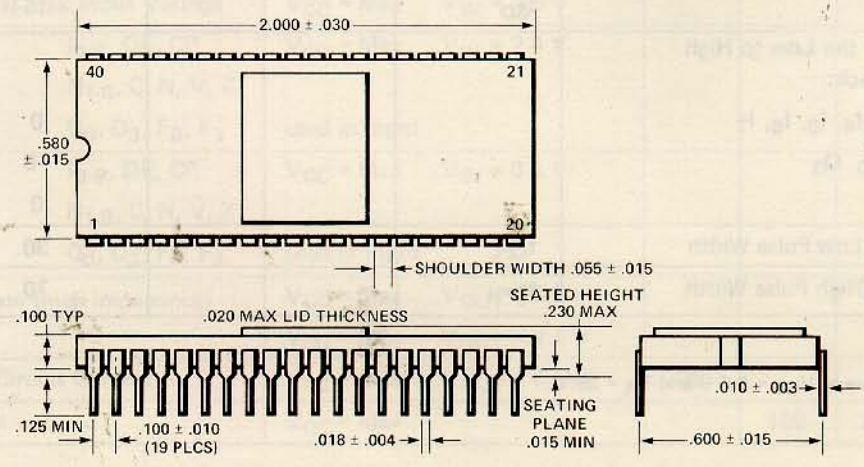
1. Typical values are at V_{CC} = 5.0 V and T_A = 25°C.



Shaded areas denote don't care conditions.

PACKAGE OUTLINE

40 Pin Ceramic (Side Braze)



θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) $\approx 35^{\circ}$C/watt.

θ_{JC} (thermal resistance from junction to case with freon as a heat sink) $\approx 20^{\circ}$C/watt.

ORDER INFORMATION—Use the Suffix "D"